Reconfigurable Gate-free Graphene Stacks at THz

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Abstract

The unique electrical properties of graphene [1] has led to the development of a wide variety of reconfigurable plasmonic THz devices, including waveguides [2, 3], resonant [4, 5] and leaky-wave antennas [6, 7] or periodic metasurfaces [8]. From the experimental point of view, single-layer graphene structures have already been characterized in the microwave [9] and terahertz [10] frequency ranges, and some promising applications, such as Faraday rotators [11] and modulators [12], have been demonstrated. However, the simple implementation and performance of these devices might be hindered by two main factors: i) the presence of a gating structure closely located to graphene, and ii) restricted control on graphene conductivity. These limitations can be overcame by using graphene stacks [3, 4, 8, 12], structures composed of two or more isolated graphene layers separated by electrically thin dielectrics, which lead to low surface resistances and may provide novel reconfiguration strategies. In the literature, this type of structures has been employed to investigate the Anderson localization of Dirac electrons at DC, which occurs in one of the graphene layers due to the "screening" effect provided by the other one [13, 14]. However, the potential of graphene stacks for THz plasmonics has not been fully considered yet.

In this context, we present here our first steps towards the experimental characterization of reconfigurable graphene stacks for THz plasmonics. Specifically, a single-layer graphene and a doublelayer graphene stack have been fabricated using CVD graphene grown on Cu foil and transferred onto a substrate using the standard wet transfer method (see details in Fig. 1). In the case of the single-layer structure (Fig.1, left), the gate voltage is applied between graphene and a polysilicon layer located beneath the dielectric insulator. In contrast, in the case of the stack (Fig. 1, right), the gate voltage is applied between the two graphene layers which compose the structure thus allowing to the graphene sheets to bias each other. Note that more advanced reconfiguration strategies can easily be developed by including additional gate voltages to this structure. The samples are then measured in transmission using terahertz time-domain spectroscopy (TDS), and the conductivity of the single-layer graphene and stack structures are retrieved using a dedicated formulation. Fig. 2 shows the real part of the extracted conductivity versus the applied voltage for both structures at the operation frequency f=1.5 THz. Results clearly confirm the reconfiguration capabilities of the samples at terahertz, demonstrating the ability of the graphene stack to self-bias without requiring additional gating components. In addition, note that the extracted conductivities possess hysteresis depending on the gate sweeping features. This phenomenon arises due to the charges and impurities trapped in the dielectric, as occurs in graphene transistors [15], and can be significantly reduced by applying an annealing process.

The results shown here will be expanded at the conference by studying the frequency dependent behaviour of the extracted conductivity, by further investigating the reconfiguration capabilities of graphene stacks when various gate voltages are considered, and by proposing a simple theoretical model able to characterize the proposed structure. The experimental results shown here are very promising for the future integration of graphene in tunable plasmonic THz devices.

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Figures



Figure 1: Single graphene layer (left column) and double-layer graphene stack (right column) structures considered in this work.



Figure 2: Measured real part of the conductivity (real part) related to the single-layer graphene (a) and doublelayer (b) graphene structures shown in Fig. 1 versus the applied gate voltage at 1.5 THz. Results clearly confirm the hysteresis behavior of graphene conductivity at terahertz. In the case of the single layer graphene, conductivity is plotted before and after applying an annealing process to the sample.